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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/610,753	07/06/00	YAMAZAKI S	SEL 195

MM91/1010
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EXAMINER	
BROCK II,P	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/10/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)

1- File Copy

Office Action Summary	Application No.	Applicant(s)	
	09/610,753	YAMAZAKI ET AL.	
	Examin r	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) *2,4-20,22,24,26 and 28-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,21,23,25 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group II and Species A in Paper No. 5 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

The applicant has failed to point out the particular claims within Group II that read on Species A. It has been determined that only claims 1, 3, 21, 23, 25 and 27 read on the elected species. Claims 2, 4 – 20, 22, 24, 26 and 28 – 52 have been withdrawn from further consideration.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show photoresist masks PM1 and PM6 as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Correction is required. While these features are pointed to in the figures they are not represented such as PM2, PM3, PM4 and PM5.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 25 and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear how the claimed semiconductor device could be a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic game machine or a projector. How could this device be a personal computer?

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto (USPAT 5323042, Matsumoto) in view of Adan et al. (USPAT 5841170, Adan) and Shimone (JPPAT 6258659).

With regard to claim 1, Matsumoto discloses in figure 1 a semiconductor device. Matsumoto discloses in figure 1 a pixel TFT (21) disposed in a pixel section, and a driver circuit comprising a p-channel TFT (23) and an n-channel TFT (22), over a substrate (11). Matsumoto discloses in figure 1 the p-channel TFT of the driver circuit comprises a channel forming region (23a) and a p-type impurity region (23c) of a fourth concentration that forms a source region or a drain region. Matsumoto discloses in figure 1 the n-channel TFT of the driver circuit comprises a channel forming region, an n-type impurity region of a first concentration (22b) which forms a LDD region that is disposed in contact with the channel forming region and an n-type impurity region (22c) of a third concentration which is disposed in the outside of the n-type impurity region of the first concentration and forms a source region of a drain region. Matsumoto does

not disclose that the LDD region partly overlaps a gate electrode (26). Adan teaches in figure 29 an LDD region (71) that partly overlaps a gate electrode (66). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the partly overlapping LDD regions of Adan in the device of Matsumoto in order to increase the breakdown voltage of the transistor as stated by Matsumoto in column 2, lines 17 – 25. Matsumoto discloses in figure 1 the pixel TFT comprises a channel forming region (21a), an n-type impurity region (21b) of a second concentration which is disclosed in contact with the channel forming region and forms a LDD region, and an n-type impurity region (21c) of the third concentration which is disposed in the outside of the n-type impurity region of the second concentration and forms a source region or a drain region. Matsumoto discloses in figure 1 a pixel electrode (32) in the pixel section has a light reflective surface, the pixel electrode is formed over an interlayer insulating film and is connected to the pixel TFT through an opening in the interlayer insulating film. Matsumoto and Adan do not disclose that the interlayer insulating film comprises an organic insulating material, and there is an opening formed in a protective insulating film comprising an inorganic insulating material in contact with the organic insulating material and disposed over a gate electrode of the pixel TFT. Shimone discloses in figure 3d a pixel electrode (106) disposed in a pixel section, the pixel electrode is formed over an interlayer insulating film (104) comprising an organic insulating material, and is connected to the pixel TFT through an opening formed in a protective insulating film (113) comprising an inorganic insulating material disposed over a gate electrode of the pixel TFT and in the interlayer insulating film formed in contact with the protective insulating film. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the organic insulating layer and inorganic protective film with a hole

therein to connect the pixel electrode to the pixel TFT of Shimone in the device of Matsumoto and Adan in order to use a material capable of photo imaging as the interlayer dielectric.

With regard to claim 25, the semiconductor device of Matsumoto, Adan and Shimone could obviously be part of a personal computer.

7. Claims 3 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Adan, Shimone and Karauchi et al. (JPPAT 9120072, Karauchi).

Claim 3 is rejected similar to claim 1 above by Matsumoto, Adan and Shimone. Matsumoto discloses in figure 1 a substrate that comprises a pixel TFT disposed in a pixel section and a p-channel TFT and an n-channel TFT of a driver circuit. Matsumoto, Adan and Shimone do not disclose a liquid crystal sandwiched between a pair of substrates. Karauchi discloses in figure 7 a liquid crystal sandwiched between a pair of substrates (111 and 91). Karauchi further discloses in figure 7 one of the substrate is stuck to the other substrate on which a transparent conductive film is formed, through at least a columnar spacer on superposition of an opening. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the dual substrates and columnar spacer of Karauchi in the device of Matsumoto, Adan and Shimone in order to create a liquid crystal display with constant distance between substrates.

With regard to claim 27, the semiconductor device of Matsumoto, Adan and Shimone could obviously be part of a personal computer.

8. Claims 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto, Adan, Shimone and Karauchi as applied to claim 3 above, and further in view of Hioki (JPPAT 8234212).

With regard to claim 21, Matsumoto, Adan, Shimone and Karauchi do not disclose a columnar spacer over the TFTs of the driver circuit. Hioki discloses in figure 1 a columnar spacer (24) formed over TFTs (22) of the driver circuit. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the columnar spacer of Hioki to cover the p-channel TFT and the n-channel TFT in the device of Matsumoto, Adan, Shimone and Karauchi in order to.

With regard to claim 22, Matsumoto, Adan, Shimone and Karauchi do not disclose a columnar spacer formed to cover at least a source wiring of the p-channel TFT and the n-channel TFT. Hioki discloses in figure 1 a columnar spacer formed to cover source wirings of TFTs. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the columnar spacer of Hioki to cover the source wirings of the p-channel TFT and the n-channel TFT in Matsumoto, Adan, Shimone and Karauchi in order to eliminate forming spacers on pixel electrodes as stated by Hioki.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yudasaka et al., Kobayashi et al., Byun et al., Yamamoto et al., Furuta, Ichikawa et al., Katayama et al. and Kawachi et al. all disclose TFTs for liquid crystal displays.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
October 3, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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